CLAIMS

What is claimed is:

1. An automated method for designing an integrated circuit (IC) design-specific cell, said method comprising the steps of:

receiving a design specification for said design-specific cell;

mapping to a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

evaluating said transistor-level representation of said design-specific cell for meeting said design specification.

2. The method of claim 1, wherein said step of evaluating comprises evaluating said transistor-level representation of said design-specific cell based on the specific design context in which said design-specific cell is to be used.

3. The method of claim 1, wherein said step of receiving comprises receiving a description of said design-specific cell.

4. The method of claim 3, wherein said description is selected from a group consisting of a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.

5. The method of claim 1, wherein said design specification is selected from the group consisting of: size (area), signal timing, transistor sizing, number of

transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof.

6. The method of claim 1, wherein said step of mapping comprises:

generating a transistor netlist based on at least one netlist generation algorithm; and

evaluating said generated transistor netlist based on at least one design specification.

7. The method of claim 1, wherein said step of mapping is based on at least one of a plurality of topology formats.

8. The method of claim 6, wherein said step of mapping further comprises optimizing transistor size for said generated transistor netlist.

9. The method of claim 1, wherein said method further comprises the step of creating at least one transistor-level redundancy for aiding in satisfying said design specification.

10. The method of claim 1, wherein said method further comprises the step of detecting an implementation weakness in a cell for implementing said IC.

11. A system for automatically designing an integrated circuit (IC) design-specific cell, said system comprising:

an interface for receiving a design specification for said design-specific cell;

means for mapping a transistor-level representation of said design-specific cell, wherein said means for mapping uses said design-specific specification as a basis for the mapping; and

means for evaluating said transistor-level representation of said design-specific cell for determining whether said transistor-level representation of said IC meets said design specification.

12. The system of claim 11, wherein said means for evaluating is capable of evaluating said transistor-level representation of said design-specific cell based on the specific design context in which said design-specific cell is to be used.

13. The system of claim 11, wherein said interface receives a description of said design-specific cell.

14. The system of claim 13, wherein said description received by said interface is selected from a group consisting of: a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.

15. The system of claim 11, wherein said means for mapping controls the mapping of said transistor-level representation on the basis of said design-specific specification selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, fault tolerance, integrity characteristics, noise characteristics, and a combination thereof.

16. The system of claim 11, wherein said means for mapping is capable of generating a transistor netlist based on at least one netlist generation algorithm;

and evaluating said generated transistor netlist based on at least one design specification.

17. The system of claim 11, wherein said means for mapping further comprises a control means for the mapping using a plurality of topology formats.

18. The system of claim 11, wherein said means for mapping further comprises a control means for optimization of transistor sizing for said generated transistor netlist.

19. The system of claim 11, wherein said system further comprises means for creating at least one transistor-level redundancy for said IC cell for aiding in meeting said design specification.

20. The system of claim 11, wherein said system further comprises means for detecting an implementation weakness in a cell for implementing said IC. .

21. A design-specific cell produced by an automated integrated circuit (IC) design process, said IC design process comprises the steps of:

receiving a design specification for said design-specific cell;

mapping a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

evaluating said transistor-level representation of said design-specific cell for meeting of said design specification.

22. The design-specific cell produced by the IC design process of claim 21, wherein said step of evaluating comprises evaluating said transistor-level representation of said design-specific cell based on the specific design context in which said design-specific cell is to be used.

23. The design-specific cell produced by the IC design process of claim 21, wherein said step of receiving comprises receiving a description of said design-specific cell.

24. The design-specific cell produced by the IC design process of claim 23, wherein said description is selected from a group consisting of: a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.

25. The design-specific cell produced by the IC design process of claim 21, wherein said design specification is selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof.

26. The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping comprises:

generating a transistor netlist based on at least one netlist generation algorithm; and

evaluating said generated transistor netlist based on at least one design specification.

27. The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping is based on at least one plurality of topology format.

28. The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping further comprises means for optimizing the transistor size for said generated transistor netlist.

29. The design-specific cell produced by the IC design process of claim 21, wherein said method further comprises the step of creating at least one transistor-level redundancy for aiding in meeting said design specification.

30. A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit (IC) design-specific cell, said storage medium comprising:

program instructions for receiving a design specification for said design-specific cell;

program instructions for mapping a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

program instructions for evaluating said transistor-level representation of said design-specific cell for satisfaction of said design specification.